



Arm® CoreSight™ ETM-M23

Revision: r0p1

Technical Reference Manual

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Issue

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Arm® CoreSight™ ETM-M23 Technical Reference Manual

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1. Introduction

1.1 Implementation obligations

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1.2 Product revision status

The r_xp_y identifier indicates the revision status of the product described in this manual, for example, $r1p2$, where:

| | |
|-------------------------|--|
| r_x | Identifies the major revision of the product, for example, $r1$. |
| p_y | Identifies the minor revision or modification status of the product, for example, $p2$. |

1.3 Intended audience

This book is written for: Designers of development tools providing support for ETM functionality. Implementation-specific behavior is described in this document. You can find complementary information in the Embedded Trace Macrocell Architecture Specification (Arm IHI 0014). Hardware and software engineers integrating the macrocell into an ASIC that includes a Cortex-M23 processor.

1.4 Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

| Convention | Use |
|----------------------------|--|
| <i>italic</i> | Citations. |
| bold | Terms in descriptive lists, where appropriate. |
| monospace | Text that you can enter at the keyboard, such as commands, file and program names, and source code. |
| monospace <u>underline</u> | A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name. |
| <and> | Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <div>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></div> |
| SMALL CAPITALS | Terms that have specific technical meanings as defined in the <i>Arm® Glossary</i> . For example, IMPLEMENTATION DEFINED , IMPLEMENTATION SPECIFIC , UNKNOWN , and UNPREDICTABLE . |



Recommendations. Not following these recommendations might lead to system failure or damage.



Requirements for the system. Not following these requirements might result in system failure or damage.



Requirements for the system. Not following these requirements will result in system failure or damage.



An important piece of information that needs your attention.



A useful tip that might make it easier, better or faster to perform a task.



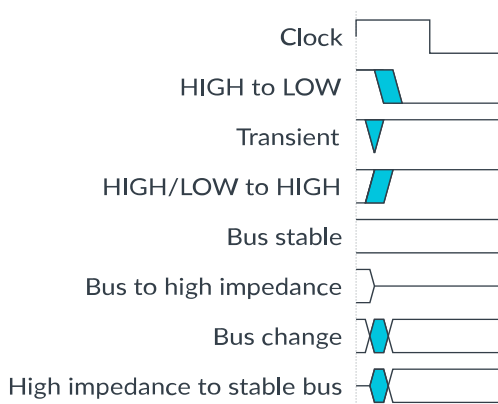
A reminder of something important that relates to the information you are reading.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

Figure 1-1: Key to timing diagram conventions



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

1.5 Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Access to Arm documents depends on their confidentiality:

- Non-Confidential documents are available at developer.arm.com/documentation. Each document link in the following tables goes to the online version of the document.
- Confidential documents are available to licensees only through the product package.

Table 1-2: Arm Publications

| Arm product resources | Document ID | Confidentiality |
|---|--------------|------------------|
| Arm®v8-M Architecture Reference Manual | Arm DDI 0553 | Non-Confidential |
| Cortex®-M23 Processor Technical Reference Manual | Arm DDI 0550 | Non-Confidential |
| Arm® Embedded Trace Macrocell Architecture Specification | Arm IHI 0014 | Non-Confidential |
| Arm® CoreSight™ Components Technical Reference Manual | Arm DDI 0314 | Non-Confidential |
| Arm® CoreSight™ Architecture Specification v2.0 | Arm IHI 0029 | Non-Confidential |
| Arm® AMBA® 5 APB Protocol Specification Version: 2.0, | Arm IHI 0024 | Non-Confidential |
| Cortex®-M23 Processor Integration and Implementation Manual | Arm DIT 0062 | Confidential |



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2. CoreSight ETM for the Cortex-M23 Introduction

It contains the following sections:

- [2.1 About the ETM-M23](#) on page 11.
- [2.2 Compliance](#) on page 11.
- [2.3 Features](#) on page 11.
- [2.4 Interfaces](#) on page 12.
- [2.5 Configurable options](#) on page 12.
- [2.6 Test features](#) on page 12.
- [2.7 Product documentation, design flow, and architecture](#) on page 12.
- [2.8 Product revisions](#) on page 13.

2.1 About the ETM-M23

The CoreSight ETM-M23 is an optional debug component that enables a debugger to reconstruct program execution. The CoreSight ETM-M23 supports only instruction trace. You can use it either with the *Trace Port Interface Unit* (TPIU), or as part of a CoreSight system.

2.2 Compliance

ETM-M23 is compatible with the CoreSight architecture.

ETM-M23 implements version 3.5 of the ETM architecture, ETMv3.5. See the *Embedded Trace Macrocell Architecture Specification* for more information.

For more information about architectural compliance, see [2.7.1 Architecture and protocol information](#) on page 13.

2.3 Features

ETM-M23 provides:

- Tracing of 16-bit and 32-bit Thumb instructions.
- Four EmbeddedICE watchpoint inputs.
- A Trace Start/Stop block with EmbeddedICE inputs.

- One reduced functions counter.
- Two external inputs.
- A 24-byte FIFO queue.
- Global 48-bit timestamping.

See the *Embedded Trace Macrocell Architecture Specification* for information about:

- The trace protocol.
- Controlling tracing using triggering and filtering resources.

2.4 Interfaces

The system connections to the ETM-M23 are supported using a *Cross Trigger Interface* (CTI):

- 0-2 external inputs.
- Trigger output.

See [2.5 Configurable options](#) on page 12 and [3.10 Interfaces](#) on page 19 for more information about the external inputs and external outputs.

The bus interface for programming ETM registers is the APB interface.

2.5 Configurable options

The ETM-M23 macrocell includes the following configuration inputs:

- The maximum number of external inputs, see [3.7 External inputs](#) on page 19.
- Whether the system supports the FIFOFULL mechanism for stalling the processor, see [Table 3-1: Cortex-M23 processor resources](#) on page 16.

2.6 Test features

The ETM-M23 does not include any specific *Design For Test* (DFT) features.

2.7 Product documentation, design flow, and architecture

This section describes the ETM-M23 books, how they relate to the design flow, and the relevant architectural standards and protocols.

See [Additional reading](#) for more information about the books described in this section.

Documentation

The ETM-M23 documentation is as follows:

Technical Reference Manual

The *Technical Reference Manual* (TRM) describes the functionality and the effects of functional options on the behavior of the ETM-M23. It is required at all stages of the design flow. Some behavior that is described in the TRM might not be relevant because of the way that the ETM-M23 is implemented and integrated.

Design flow

The ETM-M23 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following process:

1. Implementation. The implementer synthesizes the RTL, usually in combination with the processor, then places and routes the netlist to produce a hard macrocell.
2. Integration. The integrator instantiates the macrocell of the combined processor and ETM into a SoC. This includes testing its integration with the other SoC components to which it is connected.
3. Programming. The debug software developer programs the ETM and tests any trace software required for use with a SoC.

2.7.1 Architecture and protocol information

The ETM-M23 complies with, or implements, the specifications described in:

- [2.7.2 Trace macrocell](#) on page 13.
- [2.7.3 Advanced Microcontroller Bus Architecture](#) on page 13.

This TRM complements architecture reference manuals, architecture specifications, protocol specifications, and relevant external standards. It does not duplicate information from these sources.

2.7.2 Trace macrocell

The ETM-M23 implements the ETM architecture version 3.5.

See *Embedded Trace Macrocell Architecture Specification*.

2.7.3 Advanced Microcontroller Bus Architecture

This ETM-M23 complies with the *Advanced Microcontroller Bus Architecture* (AMBA) APB protocols.

See *AMBA® 5 APB Protocol Specification Version: 2.0*.

2.8 Product revisions

This section describes the differences in functionality between product revisions:

r0p0

First release.

r0p1

There are no differences in functionality for this release.

r0p1

Second release for r0p1. There are no differences in functionality for this release.

r0p1

Third release for r0p1. There are no differences in functionality for this release.

3. Functional Description

Functional Description

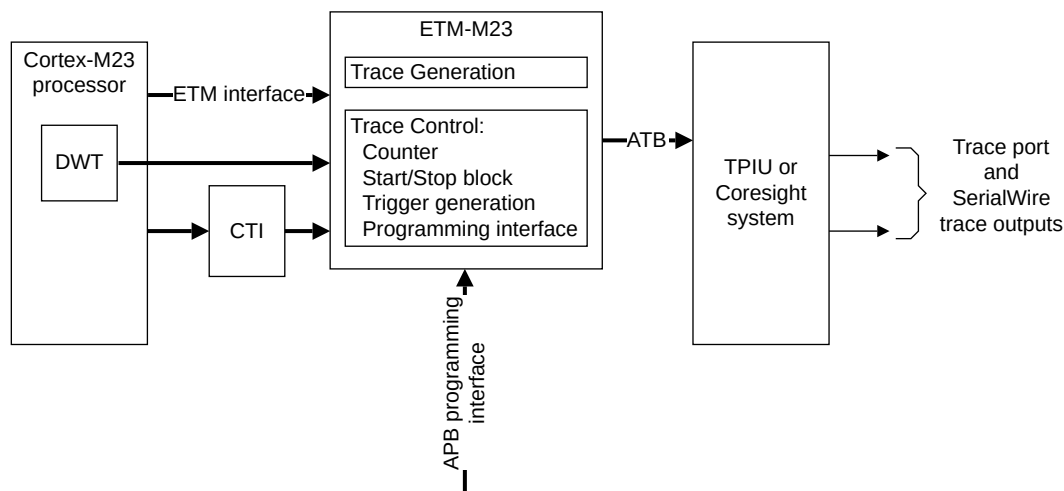
This chapter describes the interfaces, operation, clocking, and resets of the macrocell. It contains the following sections:

- [3.1 About the functions](#) on page 15.
- [3.10 Interfaces](#) on page 19.
- [3.11 Clocking and resets](#) on page 20.

3.1 About the functions

The following block diagram of the ETM shows how the ETM interfaces to the *Trace Port Interface Unit (TPIU)*.

Figure 3-1: ETM block diagram



The ETM trace output is compatible with the AMBA *Trace Bus* (ATB) protocol, irrespective of the configuration of the trace port size and trace port mode within the ETM programmers model. The TPIU exports trace information from the processor. An implementation can replace the TPIU with other CoreSight trace components.

For more information, see:

- *Cortex®-M23 Processor Technical Reference Manual*.
- *Embedded Trace Macrocell Architecture Specification*.

The ETM provides a trace ID register for systems that use multiple trace sources. You must configure this register even if only a single trace source is in use.

The following sections provide information on features of the ETM:

- [3.2 Resources](#) on page 16.
- [3.4 Timestamp format](#) on page 18.
- [3.5 Periodic synchronization](#) on page 18.
- [3.6 Data and instruction address compare resources](#) on page 18.
- [3.7 External inputs](#) on page 19.
- [3.8 Start/stop block](#) on page 19.
- [3.9 Triggering](#) on page 19.

3.2 Resources

Because the ETM does not generate data trace information, the lower bandwidth reduces the requirement for complex triggering capabilities. This means that the ETM only includes a small subset of the possible resources permitted by the ETM architecture.

The following table lists the Cortex-M23 processor resources.

Table 3-1: Cortex-M23 processor resources

| Feature | Present on ETM-M23 |
|-----------------------------------|----------------------------------|
| Architecture version | ETMv3.5 |
| Address comparator pairs | 0 |
| Data comparators | 0 |
| Context ID comparators | 0 |
| Memory Map Decoders (MMDs) | 0 |
| Counters | 1, reduced function counter only |
| Sequencer | No |
| Start/stop block | Yes |
| EmbeddedICE comparators | 4 |
| External inputs | 2 |
| External outputs | 0 |
| Extended external inputs | 0 |
| Extended external input selectors | 0 |
| FIFOFULL | Yes |
| FIFOFULL level setting | Yes |
| Branch broadcasting | Yes |
| ASIC Control Register | No |
| Data suppression | No |

| Feature | Present on ETM-M23 |
|---|--|
| Software access to registers | Yes |
| Readable registers | Yes |
| FIFO size | 24 bytes |
| Minimum ATB port size | 8 bits |
| Maximum ATB port size | 8 bits |
| Normal port mode | - |
| Normal half-rate clocking, 1:1 | Yes - asynchronous |
| Demultiplexor port mode | - |
| Demultiplexor half-rate clocking, 1:2 | No |
| Multiplexor port mode, 2:1 | No |
| 1:4 port mode | No |
| Dynamic port mode, including stalling | No. Supported by asynchronous port mode. |
| Coprocessor Register Transfer (CPRT) data | No |
| Load PC first | No |
| Fetch comparisons | No |
| Load data traced | No |

3.3 Resource identification encoding

You configure the trace enable event, timestamp event, and trigger event using the same mechanism. For each event, a 17-bit register is used to define the event. This register provides:

- Resource A, bits[6:0].
- Resource B, bits[13:7].
- A boolean function, bits[16:14].

The following table shows the encodings that are used for the boolean function.

Table 3-2: Boolean function encoding for events

| Encoding | Function |
|----------|--------------------|
| 0b000 | A |
| 0b001 | NOT(A) |
| 0b010 | A AND B |
| 0b011 | NOT(A) AND B |
| 0b100 | NOT(A) AND NOT (B) |
| 0b101 | A OR B |
| 0b110 | NOT (A) OR B |
| 0b111 | NOT (A) OR NOT (B) |

The following table shows the encodings that are used for Resource identification.

Table 3-3: Resource identification encoding

| Resource type ¹ | Index range ² | Description of resource type |
|----------------------------|--------------------------|------------------------------|
| 0b010 | 0-3 | DWT Comparator inputs (0-3) |
| 0b100 | 0 | Counter 1 at zero |
| 0b101 | 15 | Trace Start/Stop resource |
| 0b110 | 0-1 | ExtIn (0-1) |
| 0b110 | 15 | HardWired (always True) |

3.4 Timestamp format

Timestamps are encoded as 48-bit binary numbers. A system implementation can provide a timestamp count that can be used by several trace sources as an aid to correlating the trace streams.

3.5 Periodic synchronization

The ETM uses a fixed synchronization packet generation frequency of every 1024 bytes of trace.

3.6 Data and instruction address compare resources

The DWT provides four address comparators on the data bus that provide debug functionality. Within the DWT unit, you can specify the functions triggered by a match, and one of these functions is to generate an ETM match input. These inputs are presented to the ETM as embedded *In Circuit Emulator* (ICE) comparator inputs.

A single DWT resource can trigger an ETM event and also generate instrumentation trace directly from the same event.

You can configure the four DWT comparators individually to compare with the address of the current executing instruction to permit the ETM access to an instruction address compare resource. These inputs are presented to the ETM as EmbeddedICE comparator inputs. The DWT provides either one or four comparators, depending on the implementation of the processor.



Using a DWT comparator as an instruction address comparator reduces the number of available data address comparisons.

¹ For Resource A, bits[6:4]. For Resource B, bits[13:11].

² For Resource A, bits[3:0]. For Resource B, bits[10:7].

See the *Cortex®-M23 Processor Technical Reference Manual* for more information about the DWT unit.

3.7 External inputs

Two external inputs, ETMEXTIN[1:0], enable additional components to generate trigger and enable signals for the ETM.

3.8 Start/stop block

The start/stop block provides a single-bit resource that can be used as an input to other parts of the resource logic, including the trace enable logic. The start/stop block can only be controlled by using the embeddedICE inputs to the ETM. The DWT controls these inputs.

The start/stop block is set to the start state if any of the EmbeddedICE watchpoint inputs selected as start resources in ETMTESSEICR go HIGH. The start/stop block is set to the stop state if any of the EmbeddedICE watchpoint inputs selected as stop resources in ETMTESSEICR go LOW.

If bit[25] of ETMTECR1 is 1, tracing is only enabled when the start/stop block is in the start state.

Tracing is also only enabled when the result of evaluating the Trace Enable Event is TRUE. This event can be set to always be TRUE by programming a value of 0x6F to ETMTREEVR. For more information, see the *Embedded Trace Macrocell Architecture Specification*.

3.9 Triggering

The ETM provides a trigger resource that can be used to identify a point within a trace run. The generation of a trigger does not affect the tracing in any way, but the trigger is output in the trace stream, and can also be passed to other trace components or used to halt the processor. An external Trace Port Analyzer can use the trigger to determine when to start and stop capture of trace.

3.10 Interfaces

The ETM-M23 has the following external interfaces:

ATB

A 32-bit ATB provides trace output from the macrocell. See the *Arm® AMBA® 4 ATB Protocol Specification* for more information about this interface.

APB

An APB provides the control interface for the macrocell. See the *Arm® AMBA® 4 APB Protocol Specification* for more information about this interface.

CTI

Your implementation can provide a *Cross Trigger Interface* to manage the interconnection of trigger and control signals between the processor core, ETM, and TPIU.

3.11 Clocking and resets

The following sections describe the ETM-M23 clocks and resets:

- [3.11.1 ETM-M23 clock](#) on page 20.
- [3.11.2 ETM-M23 low-power control](#) on page 20.
- [3.11.3 ETM-M23 reset](#) on page 20.
- [3.11.4 Power domain](#) on page 20.

3.11.1 ETM-M23 clock

The ETM-M23 has one clock, CLK. This clock is synchronous to the FCLK input of the Cortex-M23 processor.

3.11.2 ETM-M23 low-power control

The ETM-M23 has outputs to indicate whether the debugger expects power to be maintained, and also an output to indicate when tracing is inactive. The use of these signals is **IMPLEMENTATION SPECIFIC**.

3.11.3 ETM-M23 reset

The ETM-M23 has a single reset, nDBGTMRESET, and must only be reset by a debug reset event.



The programming state must be reconfigured after a debug reset.

3.11.4 Power domain

The ETM-M23 is in the Debug power domain. The Debug power domain cannot be turned on if the system power domain is off.

4. Programmers Model

Programmers Model

This chapter describes the programmers model. It contains the following sections:

- [4.1 About the programmers model](#) on page 22.
- [4.2 Modes of operation and execution](#) on page 22.
- [4.3 Register summary](#) on page 23.
- [4.4 Register descriptions](#) on page 24.

4.1 About the programmers model

This chapter describes the mechanisms for programming the registers that are used to set up the trace and triggering facilities of the macrocell. The programmers model enables you to use the ETM registers to control the macrocell.

4.2 Modes of operation and execution

ETM-M23 implements ETMv3.5 for tracing 16-bit and 32-bit Thumb™ instructions.

The *Embedded Trace Macrocell Architecture Specification* describes the features of ETMv3.5.

See [2.3 Features](#) on page 11 for information on the trace features of the ETM-M23.

When the ETM is powered up or reset, you must program all the registers that do not have an architecturally defined reset state before you enable tracing. If you do not do so, the trace results are **UNPREDICTABLE**.

When programming the ETM registers, you must enable all changes at the same time. To enable all changes, use the Programming bit in ETMCR. See [4.4.1 Main Control Register, ETMCR](#) on page 24.

When the Programming bit is set to 0 you must not write to registers other than ETMCR, because doing so can lead to **UNPREDICTABLE** behavior.

When setting the Programming bit, you must not change any other bits of ETMCR. You must only change the value of bits other than the Programming bit of ETMCR when bit[1] of ETMSR is set to 1. Arm recommends that you use a read-modify-write procedure when changing ETMCR.

When authentication is not enabled, ETM-M23 behaves as follows:

- If non-invasive debug is not enabled, the ETM does not trace anything.

- If non-invasive secure debug is not enabled, the ETM traces Non-secure code, but when secure code is executed it is not visible.

4.3 Register summary

This section describes the ETM registers.

The following table provides cross-references to individual registers.

Table 4-1: ETM registers

| Address | Name | Reset | Type | Description |
|------------|---------------|------------|------|---|
| 0xE0041000 | ETMCR | 0x00000411 | RW | 4.4.1 Main Control Register, ETMCR on page 24 |
| 0xE0041004 | ETMCCR | 0x8C842000 | RO | 4.4.2 Configuration Code Register, ETMCCR on page 26 |
| 0xE0041008 | ETMTRIGGER | UNKNOWN | RW | Trigger Event Register |
| 0xE0041010 | ETMSR | UNKNOWN | RW | ETM Status Register |
| 0xE0041014 | ETMSCR | 0x00020D09 | RO | 4.4.3 System Configuration Register, ETMSCR on page 28 |
| 0xE0041020 | ETMTSEVR | UNKNOWN | RW | TraceEnable Event Register |
| 0xE0041024 | ETMTECR1 | UNKNOWN | RW | 4.4.4 TraceEnable Control 1 Register, ETMTECR1 on page 29 |
| 0xE0041028 | ETMFFLR | UNKNOWN | RW | FIFOFULL Level Register |
| 0xE0041140 | ETMCNTRLDVR1 | UNKNOWN | RW | Free-running counter reload value |
| 0xE00411E0 | ETMSYNCFR | 0x00000400 | RO | Synchronization Frequency Register |
| 0xE00411E4 | ETMIDR | 0x4114F251 | RO | 4.4.5 ID Register, ETMIDR on page 30 |
| 0xE00411E8 | ETMCCER | 0x18541800 | RO | 4.4.6 Configuration Code Extension Register, ETMCCER on page 31 |
| 0xE00411F0 | ETMTESSEICR | UNKNOWN | RW | 4.4.7 TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR on page 33 |
| 0xE00411F8 | ETMTSEVR | UNKNOWN | RW | Timestamp Event Register |
| 0xE0041200 | ETMTRACEIDR | 0x00000000 | RW | CoreSight Trace ID Register |
| 0xE0041208 | ETMIDR2 | 0x00000000 | RO | ETM ID Register 2 |
| 0xE0041314 | ETMPDSR | 0x00000001 | RO | 4.4.8 Device Power-Down Status Register, ETMPDSR on page 33 |
| 0xE0041EE0 | ITMISCIN | UNKNOWN | RO | 4.4.9 Integration Test Miscellaneous Inputs, ITMISCIN on page 34 |
| 0xE0041EE8 | ITTRIGOUT | UNKNOWN | WO | 4.4.10 Integration Test Trigger Out, ITTRIGOUT on page 35 |
| 0xE0041EF0 | ETM_ITATBCTR2 | UNKNOWN | RO | 4.4.11 ETM Integration Test ATB Control 2, ETM_ITATBCTR2 on page 36 |
| 0xE0041EF8 | ETM_ITATBCTRO | UNKNOWN | WO | 4.4.12 ETM Integration Test ATB Control 0, ETM_ITATBCTRO on page 36 |
| 0xE0041F00 | ETMITCTRL | 0x00000000 | RW | Integration Mode Control Register |
| 0xE0041FA0 | ETMCLAIMSET | UNKNOWN | RW | Claim Tag Set Register |
| 0xE0041FA4 | ETMCLAIMCLR | UNKNOWN | RW | Claim Tag Clear Register |
| 0xE0041FB0 | ETMLAR | UNKNOWN | RW | Lock Access Register |
| 0xE0041FB4 | ETMLSR | UNKNOWN | RO | Lock Status Register |
| 0xE0041FB8 | ETMAUTHSTATUS | UNKNOWN | RO | Authentication Status Register |
| 0xE0041FCC | ETMDEVTYPE | 0x00000013 | RO | CoreSight Device Type Register |
| 0xE0041FD0 | ETMPIDR4 | 0x00000004 | RO | Peripheral Identification Registers |
| 0xE0041FD4 | ETMPIDR5 | 0x00000000 | RO | |

| Address | Name | Reset | Type | Description |
|------------|-----------------------|------------|------|------------------------------------|
| 0xE0041FD8 | ETMPIDR6 | 0x00000000 | RO | |
| 0xE0041FDC | ETMPIDR7 | 0x00000000 | RO | |
| 0xE0041FE0 | ETMPIDR0 | 0x00000020 | RO | |
| 0xE0041FE4 | ETMPIDR1 | 0x000000BD | RO | |
| 0xE0041FE8 | ETMPIDR2 ³ | 0x0000001B | RO | |
| 0xE0041FEC | ETMPIDR3 | 0x00000000 | RO | |
| 0xE0041FF0 | ETMCIDR0 | 0x0000000D | RO | Component Identification Registers |
| 0xE0041FF4 | ETMCIDR1 | 0x00000090 | RO | |
| 0xE0041FF8 | ETMCIDR2 | 0x00000005 | RO | |
| 0xE0041FFC | ETMCIDR3 | 0x000000B1 | RO | |

For more information on the ETM registers, see the *Arm® Embedded Trace Macrocell Architecture Specification*.

4.4 Register descriptions

The following sections describe registers which have an implementation that is specific to this product.

Other registers are described in the *Embedded Trace Macrocell Architecture Specification*.

4.4.1 Main Control Register, ETMCR

The ETMCR characteristics are:

Purpose

Controls general operation of the ETM, such as whether tracing is enabled.

Usage constraints

There are no usage constraints.

Configurations

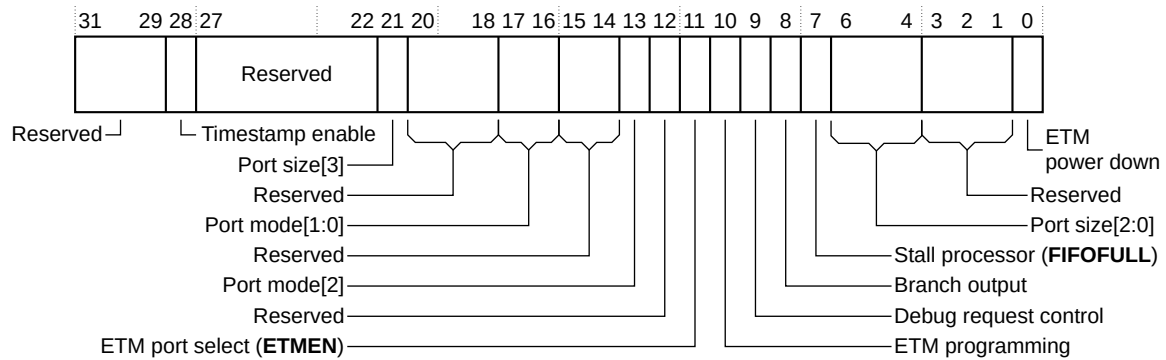
This register is only available if the processor is configured to use the ETM.

Attributes

See the ETM register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMCR bit assignments.

³ Bits[7:4] are 0x1.

Figure 4-1: ETMCR bit assignments

The following table shows the ETMCR bit assignments.

Table 4-2: ETMCR bit assignments

| Bits | Name | Function |
|---------|------------------|--|
| [31:29] | - | Reserved, Read As Zero. |
| [28] | Timestamp enable | When set, this bit enables timestamping. An ETM reset sets this bit to 0. |
| [27:22] | - | Reserved, Read As Zero. |
| [21] | Port size[3] | This bit is implemented but has no function. An ETM reset sets this bit to 0. |
| [20:18] | - | Reserved. |
| [17:16] | Port mode[1:0] | These bits are implemented but have no function. An ETM reset sets these bits to 0. |
| [15:14] | - | Reserved. |
| [13] | Port mode[2] | This bit is implemented but has no function. An ETM reset sets this bit to 0. |
| [12] | - | Reserved. |
| [11] | ETM port select | This bit can be used to control other trace components in an implementation. The possible values are: 0 ETMEN is LOW. 1 ETMEN is HIGH. This bit must be set by the trace software tools to ensure that trace output is enabled from this ETM. An ETM reset sets this bit to 0. |

| Bits | Name | Function |
|-------|-----------------------|--|
| [10] | ETM programming | <p>This bit must be set to 1 at the start of the ETM programming sequence. Tracing is prevented while this bit is set to 1.</p> <p>An ETM reset sets this bit to 0b1.</p> |
| [9] | Debug request control | <p>When set to 1 and the trigger event occurs, the ETMDBGRQ output is asserted until HALTED is observed. This enables the Arm processor to be forced into Debug state.</p> <p>An ETM reset sets this bit to 0.</p> |
| [8] | Branch output | <p>When set to 1, all branch addresses are output, even if the branch was because of a direct branch instruction. Setting this bit enables reconstruction of the program flow without having access to the memory image of the code being executed.</p> <p>When this bit is set to 1, more trace data is generated, and this can affect the performance of the trace system. Information about the execution of a branch is traced regardless of the state of this bit.</p> <p>An ETM reset sets this bit to 0.</p> |
| [7] | Stall processor | <p>The FIFOFULL output can be used to stall the processor to prevent overflow. The FIFOFULL output is only enabled when the stall processor bit is set to 1. When the bit is 0, the FIFOFULL output always remains LOW and the FIFO overflows if there are too many trace packets. If overflow does occur, trace resumes without corruption when the FIFO has drained.</p> <p>An ETM reset sets this bit to 0.</p> <p>For information about the interaction of this bit with the ETMFFLR register, see the <i>Embedded Trace Macrocell Architecture Specification</i>.</p> |
| [6:4] | Port size[2:0] | <p>The ETM-M23 has no influence over the external pins that are used for trace. These bits are implemented but not used.</p> <p>An ETM reset sets these bits to 0b001.</p> |
| [3:1] | - | Reserved. |
| [0] | ETM power down | <p>This bit can be used by an implementation to control if the ETM is in a low-power state. This bit must be cleared by the trace software tools at the beginning of a debug session.</p> <p>When this bit is set to 1, writes to some registers and fields might be ignored. You can always write to the following registers and fields:</p> <ul style="list-style-type: none"> ETMCR bit[0]. ETMLAR. ETMCLAIMSET register. ETMCLAIMCLR register. <p>When the ETMCR is written with this bit set to 1, bits other than bit[0] might be ignored.</p> <p>An ETM reset sets this bit to 1.</p> |

4.4.2 Configuration Code Register, ETMCCR

The ETM Configuration Code Register characteristics are:

Purpose

Enables software to read the implementation-specific configuration of the ETM.

Usage constraints

There are no usage constraints.

Configurations

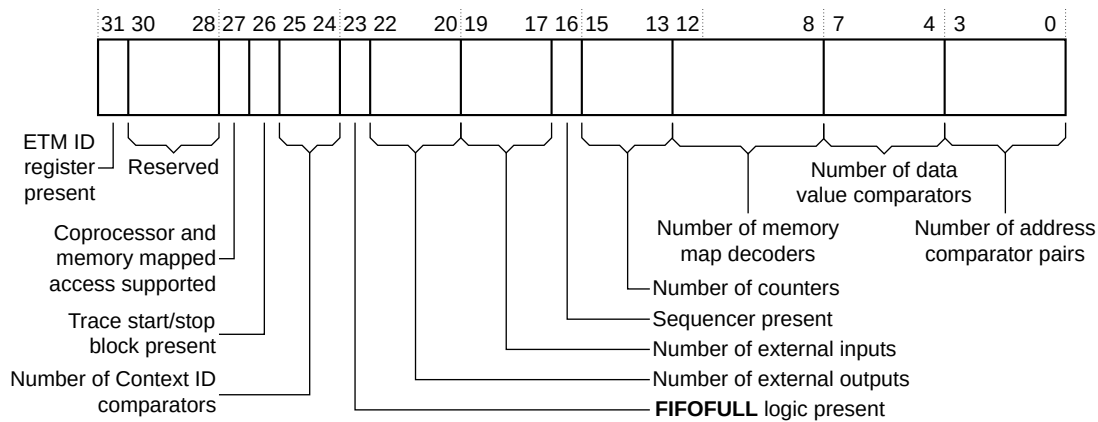
This register is only available if the processor is configured to use the ETM.

Attributes

See the ETM register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMCCR bit assignments.

Figure 4-2: ETMCCR bit assignments



The following table shows the ETMCCR bit assignments.

Table 4-3: ETMCCR bit assignments

| Bits | Name | Function |
|---------|----------------------------------|--|
| [31] | ETM ID register present | The value of this bit is 1, indicating that the ETMIDR, register 0x79, is present and defines the ETM architecture version in use. |
| [30:28] | - | Reserved. |
| [27] | Coprocessor and memory access | The value of this bit is 1, indicating that memory-mapped access to registers is supported. |
| [26] | Trace start/stop block present | The value of this bit is 1, indicating that the Trace start/stop block is present. |
| [25:24] | Number of Context ID comparators | The value of these bits is 0b00, indicating that Context ID comparators are not implemented. |

| Bits | Name | Function |
|---------|------------------------------------|--|
| [23] | FIFOFULL logic present | The value of this bit is 1, indicating that FIFOFULL logic is present in the ETM. To use FIFOFULL the system must also support the function, as indicated by bit[8] of ETMSCR, see 4.4.3 System Configuration Register, ETMSCR on page 28. |
| [22:20] | Number of external outputs | The value of these bits is 0b000, indicating that no external outputs are supported. |
| [19:17] | Number of external inputs | The value of these bits is between 0b000 and 0b010, indicating the number of external inputs, from 0-2, implemented in the system. |
| [16] | Sequencer present | The value of this bit is 0, indicating that the sequencer is not implemented. |
| [15:13] | Number of counters | The value of these bits is 0b001, indicating that one counter is implemented. |
| [12:8] | Number of memory map decoders | The value of these bits is 0b00000, indicating that memory map decoder inputs are not implemented. |
| [7:4] | Number of data value comparators | The value of these bits is 0b0000, indicating that data value comparators are not implemented. |
| [3:0] | Number of address comparator pairs | The value of these bits is 0b0000, indicating that address comparator pairs are not implemented. |

4.4.3 System Configuration Register, ETMSCR

The ETMSCR characteristics are:

Purpose

Shows the ETM features supported by the implementation of the ETM macrocell.

Usage constraints

There are no usage constraints.

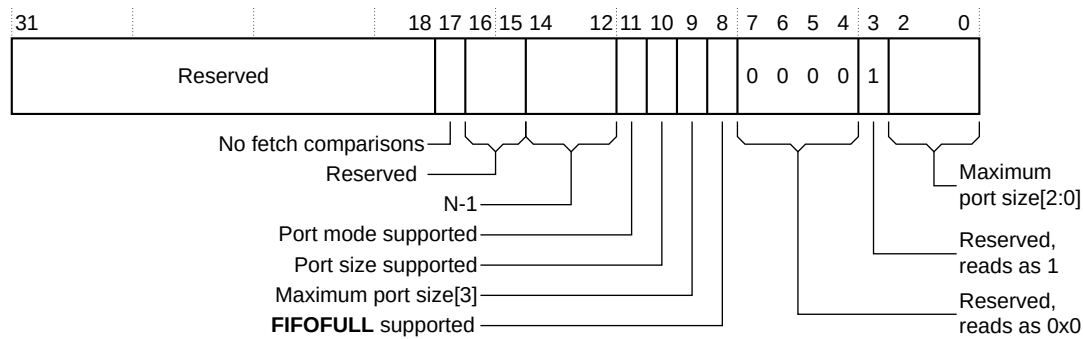
Configurations

This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMSCR bit assignments.

Figure 4-3: ETMSCR bit assignments

The following table shows the ETMSCR bit assignments.

Table 4-4: ETMSCR bit assignments

| Bits | Name | Function |
|---------|------------------------|--|
| [31:18] | - | Reserved. |
| [17] | No Fetch comparisons | The value of this bit is 1, indicating that fetch comparisons are not implemented. |
| [16:15] | - | Reserved. |
| [14:12] | N-1 | These bits indicate the number of supported processors, N, minus 1. The value of these bits is 0b000, indicating that there is only one processor connected. |
| [11] | Port mode supported | This bit reads as 1 if the currently selected port mode is supported. This has no effect on the TPIU trace port. |
| [10] | Port size supported | This bit reads as 1 if the currently selected port size is supported. This has no effect on the TPIU trace port. |
| [9] | Maximum port size[3] | Maximum ETM port size bit[3]. This bit is used with bits[2:0]. Its value is 0. This has no effect on the TPIU trace port. |
| [8] | FIFOFULL supported | The value of this bit is 1, indicating that FIFOFULL is supported. This bit is used with bit[23] of the ETMCCR. |
| [7:4] | - | Reserved, Read As Zero. |
| [3] | - | Reserved, Read As One. |
| [2:0] | Maximum port size[2:0] | Maximum ETM port size bits[2:0]. These bits are used with bit[9]. The value of these bits is 0b001. |

4.4.4 TraceEnable Control 1 Register, ETMTECR1

The ETMTECR1 characteristics are:

Purpose

Enables the start/stop logic that is used for trace enable.

Usage constraints

There are no usage constraints.

Configurations

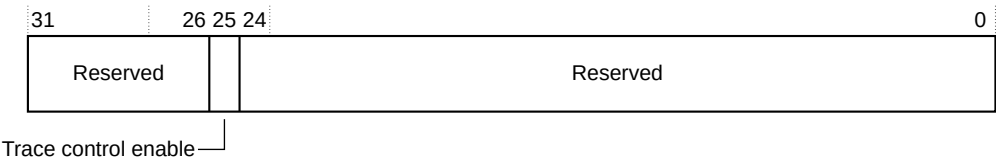
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMTECR1 bit assignments.

Figure 4-4: ETMTECR1 bit assignments



The following table shows the ETMTECR1 bit assignments.

Table 4-5: ETMTECR1 bit assignments

| Bits | Name | Function |
|---------|----------------------|---|
| [31:26] | - | Reserved. |
| [25] | Trace control enable | Trace start/stop enable. The possible values of this bit are: 0 Tracing is unaffected by the trace start/stop logic. 1 Tracing is controlled by the trace on and off addresses that are configured for the trace start/stop logic. The trace start/stop resource, resource 0x5F, is unaffected by the value of this bit. |
| [24:0] | - | Reserved. |

4.4.5 ID Register, ETMIDR

The ETMIDR characteristics are:

Purpose

Holds the ETM architecture variant, and defines the programmers model for the ETM.

Usage constraints

There are no usage constraints.

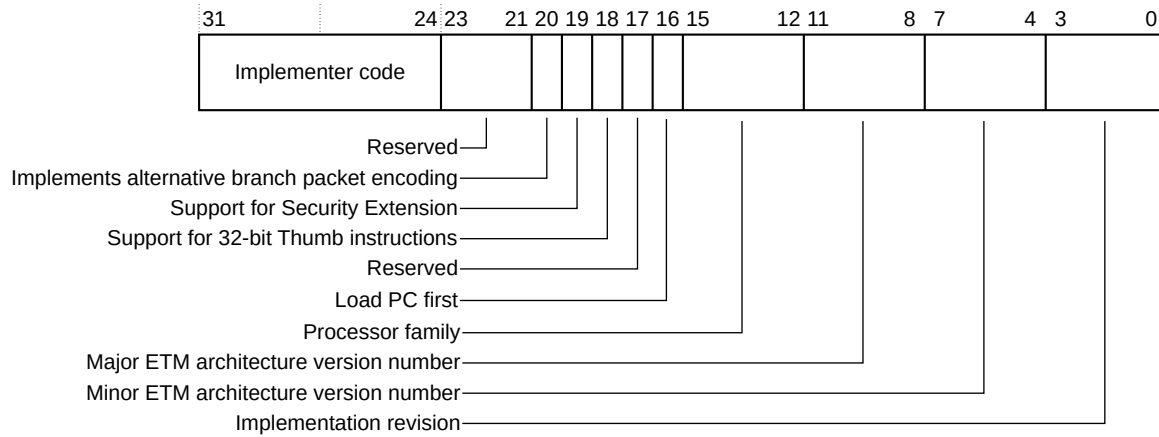
Configurations

This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMIDR bit assignments.

Figure 4-5: ETMIDR bit assignments

The following table shows the ETMIDR bit assignments.

Table 4-6: ETMIDR bit assignments

| Bits | Name | Function |
|---------|----------------------------------|---|
| [31:24] | Implementer code | These bits identify Arm as the implementer of the processor. The value of these bits is 0b1000001. |
| [23:21] | - | Reserved. |
| [20] | Branch packet encoding | The value of this bit is 1, indicating that alternative branch packet encoding is implemented. |
| [19] | Security Extension support | The value of this bit is 0, indicating that the ETM behaves as if the processor is in Secure state always. |
| [18] | 32-bit Thumb instruction tracing | The value of this bit is 1, indicating that a 32-bit Thumb instruction is traced as a single instruction. |
| [17] | - | Reserved. |
| [16] | Load PC first | The value of this bit is 0, indicating that data tracing is not supported. |
| [15:12] | Processor family | The value of these bits is 0b1111, indicating that the processor family is not identified in this register. |
| [11:8] | Major ETM architecture version | The value of these bits is 0b0010, indicating major architecture version number 3, ETMv3. |
| [7:4] | Minor ETM architecture version | The value of these bits is 0b0101, indicating minor architecture version number 5. |
| [3:0] | Implementation revision | The value of these bits is 0b0001, indicating implementation revision, 1. |

4.4.6 Configuration Code Extension Register, ETMCCER

The ETMCCER characteristics are:

Purpose

Holds ETM configuration information in addition to that in the ETMCCR. See [4.4.2 Configuration Code Register, ETMCCR](#) on page 26.

Usage constraints

There are no usage constraints.

Configurations

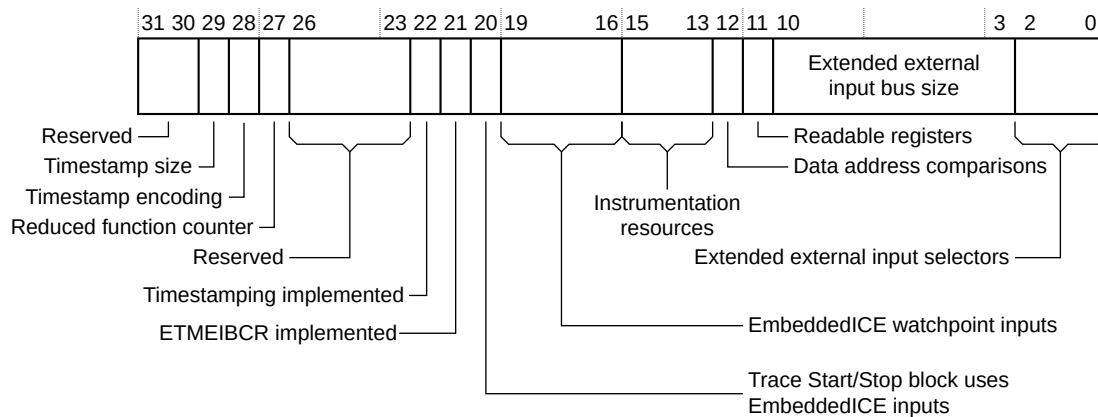
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMCCER bit assignments.

Figure 4-6: ETMCCER bit assignments



The following table shows the ETMCCER bit assignments.

Table 4-7: ETMCCER bit assignments

| Bits | Name | Function |
|---------|---|---|
| [31:30] | - | Reserved, Read As Zero. |
| [29] | Timestamp size | Set to 0 to indicate a size of 48 bits. |
| [28] | Timestamp encoding | Set to 1 to indicate that the timestamp is encoded as a natural binary number. |
| [27] | Reduced function counter | Set to 1 to indicate that Counter 1 is a reduced function counter. |
| [26:23] | - | Reserved, Read As Zero. |
| [22] | Timestamping implemented | This bit is set to 1, indicating that timestamping is implemented. |
| [21] | EmbeddedICE behavior control implemented | The value of this bit is 0, indicating that the ETMEIBCR is not implemented. For more information on EmbeddedICE behavior, see the <i>Embedded Trace Macrocell Architecture Specification</i> . |
| [20] | Trace Start/Stop block uses EmbeddedICE watchpoint inputs | The value of this bit is 1, indicating that the Trace Start/Stop block uses the EmbeddedICE watchpoint inputs. |
| [19:16] | EmbeddedICE watchpoint inputs | The value of these bits is 0b0100, indicating that the number of EmbeddedICE watchpoint inputs that are implemented is four. These inputs come from the DWT. |
| [15:13] | Instrumentation resources | The value of these bits is 0b000, indicating that no Instrumentation resources are supported. |
| [12] | Data address comparisons | The value of this bit is 1, indicating that data address comparisons are not supported. |
| [11] | Readable registers | The value of this bit is 1, indicating that all registers are readable. |

| Bits | Name | Function |
|--------|-----------------------------------|--|
| [10:3] | Extended external input bus size | The value of these bits is 0, indicating that the extended external input bus is not implemented. |
| [2:0] | Extended external input selectors | The value of these bits is 0, indicating that extended external input selectors are not implemented. |

4.4.7 TraceEnable Start/Stop EmbeddedICE Control Register, ETMTESSEICR

The ETMTESSEICR characteristics are:

Purpose

Specifies the EmbeddedICE watchpoint comparator inputs that are used to control the start/stop resource.

Usage constraints

There are no usage constraints.

Configurations

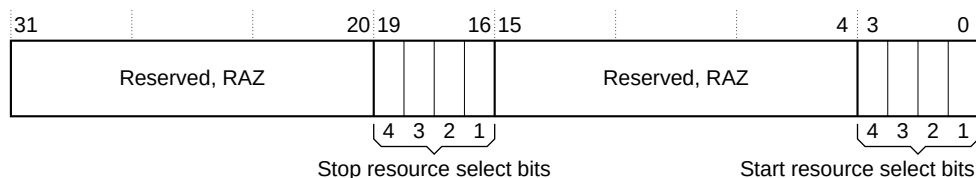
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMTESSEICR bit assignments.

Figure 4-7: ETMTESSEICR bit assignments



The following table shows the ETMTESSEICR bit assignments.

Table 4-8: ETMTESSEICR bit assignments

| Bits | Name | Function |
|---------|-----------------------|---|
| [31:20] | - | Reserved, Read As Zero. |
| [19:16] | Stop resource select | Setting any of these bits to 1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable stop resource. Bit[16] corresponds to input 1, bit[17] corresponds to input 2, bit[18] corresponds to input 3, and bit[19] corresponds to input 4. |
| [15:4] | - | Reserved, Read As Zero. |
| [3:0] | Start resource select | Setting any of these bits to 1 selects the corresponding EmbeddedICE watchpoint input as a TraceEnable start resource. Bit[0] corresponds to input 1, bit[1] corresponds to input 2, bit[2] corresponds to input 3, and bit[3] corresponds to input 4. |

4.4.8 Device Power-Down Status Register, ETMPDSR

The ETMPDSR characteristics are:

Purpose

Indicates the powerdown status of the ETM.

Usage constraints

There are no usage constraints.

Configurations

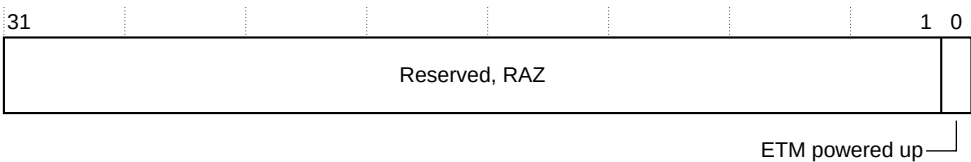
This register is only available if the processor is configured to use an ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETMPDSR bit assignments.

Figure 4-8: ETMPDSR bit assignments



The following table shows the ETMPDSR bit assignments.

Table 4-9: ETMPDSR bit assignments

| Bits | Name | Function |
|--------|----------------|---|
| [31:1] | - | Reserved, Read As Zero. |
| [0] | ETM powered up | The value of this bit indicates whether you can access the ETM Trace Registers. The value of this bit is always 1, indicating that the ETM Trace Registers can be accessed. |

4.4.9 Integration Test Miscellaneous Inputs, ITMISCIN

The ITMISCIN characteristics are:

Purpose

Integration test.

Usage constraints

There are no usage constraints.

Configurations

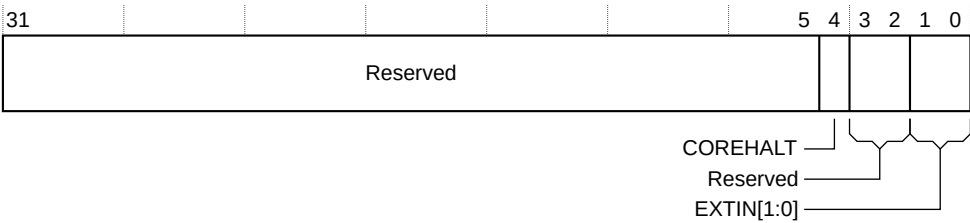
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ITMISCIN bit assignments.

Figure 4-9: ITMISCIN bit assignments



The following table shows the ITMISCIN bit assignments.

Table 4-10: ITMISCIN bit assignments

| Bits | Name | Function |
|--------|------------|--|
| [31:5] | - | Reserved. |
| [4] | COREHALT | A read of this bit returns the value of the COREHALT input pin. |
| [3:2] | - | Reserved. |
| [1:0] | EXTIN[1:0] | A read of these bits returns the value of the EXTIN[1:0] input pins. |

4.4.10 Integration Test Trigger Out, ITTRIGOUT

The ITMISCIN characteristics are:

Purpose

Integration test.

Usage constraints

You must set bit[0] of ETMITCTRL to use this register.

Configurations

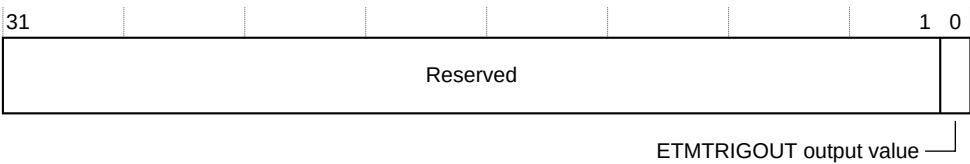
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ITTRIGOUT bit assignments.

Figure 4-10: ITTRIGOUT bit assignments



The following table shows the ITTRIGOUT bit assignments.

Table 4-11: ITTRIGOUT bit assignments

| Bits | Name | Function |
|--------|----------------------|---|
| [31:1] | - | Reserved. |
| [0] | TRIGGER output value | A write to this bit sets the ETMTRIGOUT output. |

4.4.11 ETM Integration Test ATB Control 2, ETM_ITATBCTR2

The ETM_ITATBCTR2 characteristics are:

Purpose

Integration test.

Usage constraints

You must set bit[0] of ETMITCTRL to use this register.

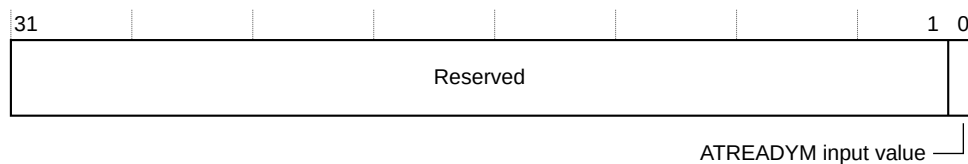
Configurations

This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETM_ITATBCTR2 bit assignments.

Figure 4-11: ETM_ITATBCTR2 bit assignments

The following table shows the ETM_ITATBCTR2 bit assignments.

Table 4-12: ETM_ITATBCTR2 bit assignments

| Bits | Name | Function |
|--------|----------------------|---|
| [31:1] | - | Reserved. |
| [0] | ATREADYM input value | A read of this bit returns the value of the ETM ATREADYM input. |

4.4.12 ETM Integration Test ATB Control 0, ETM_ITATBCTR0

The ETM_ITATBCTR0 characteristics are:

Purpose

Integration test.

Usage constraints

You must set bit[0] of ETMITCTRL to use this register.

Configurations

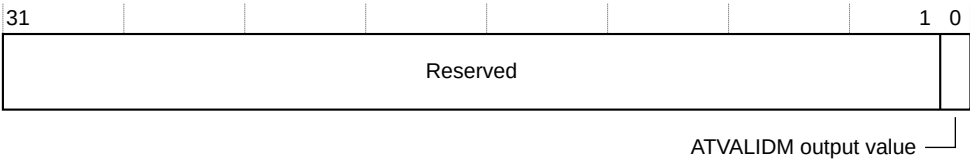
This register is only available if the processor is configured to use the ETM.

Attributes

See the register summary in [Table 4-1: ETM registers](#) on page 23.

The following figure shows the ETM_ITATBCTRO bit assignments.

Figure 4-12: ETM_ITATBCTRO bit assignments



The followig table shows the ETM_ITATBCTRO bit assignments.

Table 4-13: ETM_ITATBCTRO bit assignments

| Bits | Name | Function |
|--------|-----------------------|--|
| [31:1] | - | Reserved. |
| [0] | ATVALIDM output value | A write to this bit sets the value of the ETM ATVALIDM output. |

Appendix A Revisions

This appendix describes the technical changes between released issues of this book.

Table A-1: Issue A

| Change | Location | Affects |
|---------------|----------|---------|
| First release | - | - |

Table A-2: Differences between issue A and issue B

| Change | Location | Affects |
|--|--|---------|
| Updated the ETMIDR register | 4.4.5 ID Register, ETMIDR on page 30 | r0p1 |
| Removed the Signal Descriptions Appendix | - | r0p1 |

Table A-3: Differences between issue B and issue C

| Change | Location | Affects |
|------------------------------------|---|---------|
| Changed product name to Cortex-M23 | - | r0p1 |
| Added the timestamp input width | 2.3 Features on page 11 | r0p1 |

Table A-4: Difference between issue C and D

| Change | Location | Affects |
|--------------------------------------|---|---------|
| Updated ETMIDR and ETMCCR registers | 4.3 Register summary on page 23 | r0p1 |
| Updated the reset value for ETMPIDR2 | 4.3 Register summary on page 23 | r0p1 |